WHAT IS CLAIMED IS:

Sub A2

1. A filter circuit for use with a bit pump having a transmit and receive path, comprising:

a noise prediction equalizer configured to generate a noise prediction equalizer coefficient during activation of said bit pump to reduce an intersymbol interference associated with a receive signal propagating along said receive path; and

a decision feedback equalizer configured to generate a decision feedback equalizer coefficient during said activation of said bit pump to reduce said intersymbol interference associated with said receive signal, said noise prediction equalizer adapted to be concatenated with said decision feedback equalizer during showtime of said bit pump to form a precoder associated with said transmit path.

2. The filter circuit as recited in Claim 1 wherein said noise prediction equalizer and said decision feedback equalizer are couplable to a feed forward equalizer during said activation of said bit pump.

3. The filter circuit as recited in Claim 1 wherein said noise prediction equalizer and said decision feedback equalizer are couplable to a slicer during said activation of said bit pump.

4. The filter circuit as recited in Claim 1 wherein each of said noise prediction equalizer and said decision feedback equalizer comprise delay lines associated therewith.

5. The filter circuit as recited in Claim 1 wherein said noise prediction equalizer and said decision feedback equalizer comprise noise prediction equalizer and decision feedback equalizer coefficient arrays respectively associated therewith.

6. The filter circuit as recited in Claim 1 wherein said precoder is a Tomlinson-Harashima precoder.

7. The filter circuit as recited in Claim 1 wherein said precoder comprises a plurality of taps.

8. A method of configuring a filter circuit for use with a bit pump having a transmit and receive path, comprising:

generating a noise prediction equalizer coefficient with a noise prediction equalizer during activation of said bit pump to reduce an intersymbol interference associated with a receive signal propagating along said receive path;

generating a decision feedback equalizer coefficient with a decision feedback equalizer during said activation of said bit pump to reduce said intersymbol interference associated with said receive signal; and

concatenating said noise prediction equalizer with said decision feedback equalizer during showtime of said bit pump to form a precoder associated with said transmit path.

9. The method as recited in Claim 8 further comprising coupling said noise prediction equalizer and said decision feedback equalizer to a feed forward equalizer during said activation of said bit pump.

10. The method as recited in Claim 8 further comprising coupling said noise prediction equalizer and said decision feedback equalizer to a slicer during said activation of said bit pump.

11. The method as recited in Claim 8 wherein each of said noise prediction equalizer and said decision feedback equalizer comprise delay lines associated therewith.

12. The method as recited in Claim 8 wherein said noise prediction equalizer and said decision feedback equalizer comprise noise prediction equalizer and decision feedback equalizer coefficient arrays respectively associated therewith.

13. The method as recited in Claim 8 wherein said precoder is a Tomlinson-Harashima precoder.

14. The method as recited in Claim 8 wherein said precoder comprises a plurality of taps.

15. A bit pump having a transmit and receive path, comprising:

a modulator, coupled to said transmit path, that reduces a noise associated with a transmit signal propagating along said transmit path;

an analog-to-digital converter, coupled to said receive path, that converts a receive signal received at said bit pump into a digital format;

a decimator, coupled to said analog-to-digital converter, that downsamples said receive signal propagating along said receive path;

a filter circuit, including:

a noise prediction equalizer that generates a noise prediction equalizer coefficient during activation of said bit pump to reduce an intersymbol interference associated with said receive signal, and

a decision feedback equalizer that generates a decision feedback equalizer coefficient during said activation of said bit pump to reduce said intersymbol interference associated with said receive signal, said noise prediction equalizer being concatenated with said decision feedback equalizer during showtime of said bit pump to form a precoder associated with said transmit path; and

an echo canceling system, coupled between said transmit and receive path, that attenuates an echo in said receive signal.

16. The bit pump as recited in Claim 15 further comprising a feed forward equalizer coupled to said noise prediction equalizer and said decision feedback equalizer during said activation of said bit pump.

17. The bit pump as recited in Claim 15 further comprising a slicer coupled to said noise prediction equalizer and said decision feedback equalizer during said activation of said bit pump.

18. The bit pump as recited in Claim 15 wherein each of said noise prediction equalizer and said decision feedback equalizer comprise delay lines associated therewith.

19. The bit pump as recited in Claim 15 wherein said noise prediction equalizer and said decision feedback equalizer comprise noise prediction equalizer and decision feedback equalizer coefficient arrays respectively associated therewith.

20. The bit pump as recited in Claim 15 wherein said precoder is a Tomlinson-Harashima precoder.

A2 cont.

21. The bit pump as recited in Claim 15 wherein said precoder comprises a plurality of taps.

22. A transceiver, comprising:

a framer that formats signals within said transceiver;

a bit pump coupled to said framer and having a transmit and receive path, including:

a modulator, coupled to said transmit path, that reduces a noise associated with a transmit signal propagating along said transmit path;

an analog-to-digital converter, coupled to said receive path, that converts a receive signal received at said bit pump into a digital format;

a decimator, coupled to said analog-to-digital converter, that downsamples said receive signal propagating along said receive path;

a filter circuit, including:

a noise prediction equalizer that generates a noise prediction equalizer coefficient during activation of said bit pump to reduce an intersymbol interference associated with said receive signal, and

a decision feedback equalizer that generates a decision feedback equalizer coefficient during said activation of said bit pump to reduce said intersymbol interference associated with said receive signal, said noise prediction equalizer being concatenated with said

decision feedback equalizer during showtime of said bit pump to form a precoder associated with said transmit path; and

an echo canceling system, coupled between said transmit and receive path, that attenuates an echo in said receive signal; and

a controller that controls an operation of said framer and said bit pump.

Ag Cont.

23. The transceiver as recited in Claim 22 wherein said bit pump further comprises a feed forward equalizer coupled to said noise prediction equalizer and said decision feedback equalizer during said activation of said bit pump.

24. The transceiver as recited in Claim 22 wherein said bit pump further comprises a slicer coupled to said noise prediction equalizer and said decision feedback equalizer during said activation of said bit pump.

25. The transceiver as recited in Claim 22 wherein each of said noise prediction equalizer and said decision feedback equalizer comprise delay lines associated therewith.

26. The transceiver as recited in Claim 22 wherein said noise prediction equalizer and said decision feedback equalizer comprise noise prediction equalizer and decision feedback equalizer coefficient arrays respectively associated therewith.

27. The transceiver as recited in Claim 22 wherein said precoder is a Tomlinson-Harashima precoder.

28. The transceiver as recited in Claim 22 wherein said precoder comprises a plurality of taps.